A Study of Low-IF RF CMOS Mixers

A Thesis Proposal

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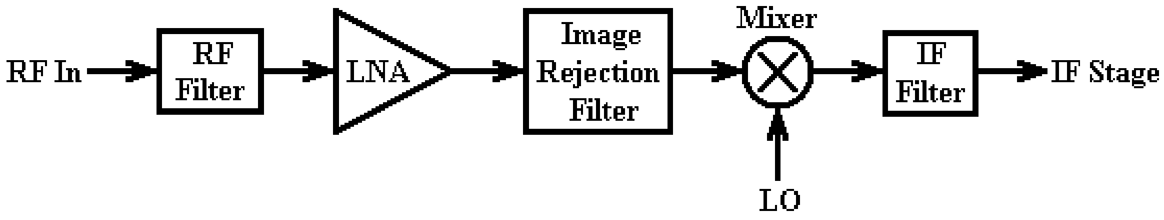
Outline

- Introduction
- Review of Related Literature
- Methodology
- Schedule
- Summary

Introduction

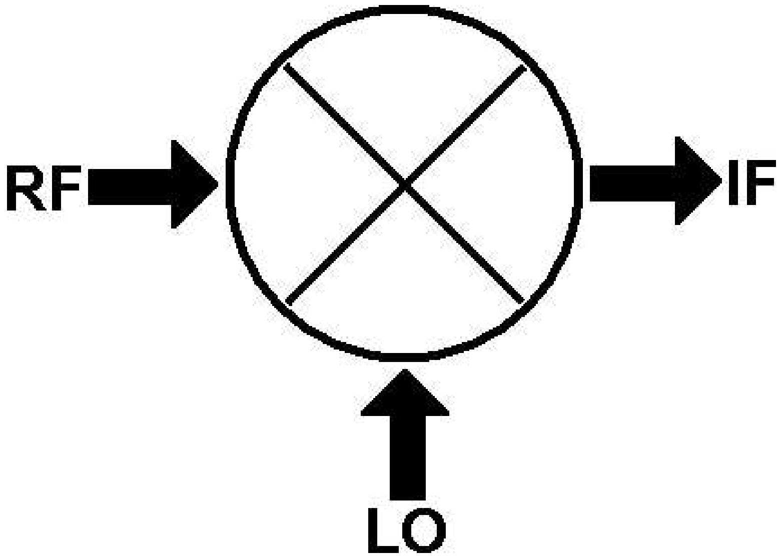
- Wireless Technology – mobile phones, IEEE802.11 standards
- Higher performance of RF circuit design tools
- RF CMOS IC – lower cost and single-chip implementation of circuits
- RF Section – critical block in most communication systems

Receiver



- Blocks
  - Filters, LNA, Mixer
- Architectures
  - High-IF, Zero-IF, Low-IF

Mixer

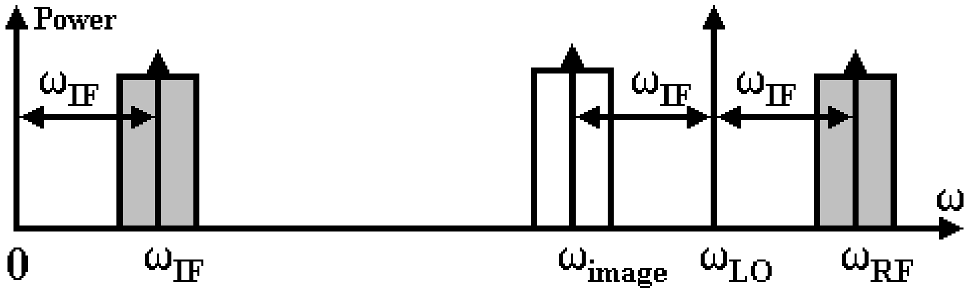


$$V_{RF} = A\cos(\omega_{RF})t \qquad V_{LO} = B\cos(\omega_{LO})t$$

$$V_{IF} = \frac{AB}{2}[\cos(\omega_{RF}+\omega_{LO})t + \cos(\omega_{RF}-\omega_{LO})t]$$

- Ports
  - Radio Frequency (RF)
    - 2.402 GHz
  - Local Oscillator Frequency (LO)
    - 2.4 GHZ
  - Intermediate Frequency (IF)
    - 2 MHz

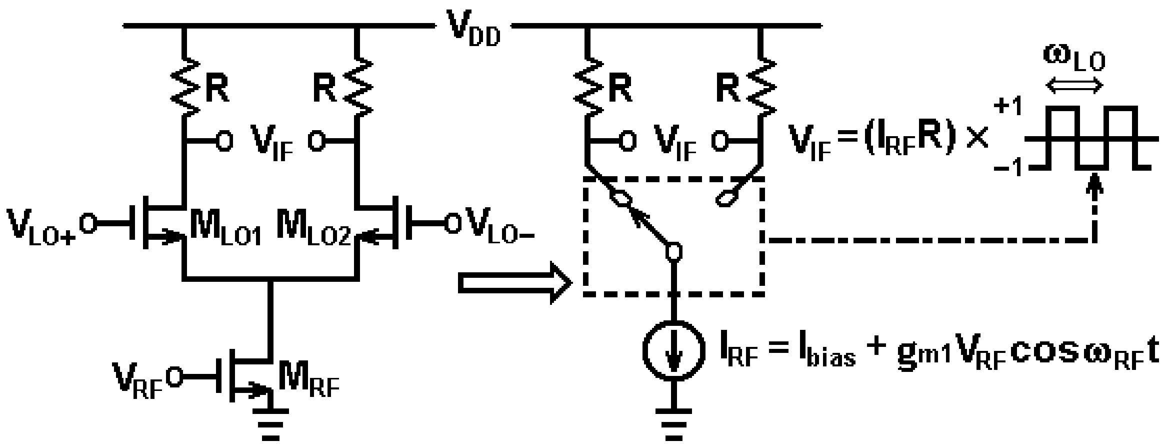
Image Frequency



$$\omega_{IF} = \omega_{RF} - \omega_{LO} \qquad \omega_{IF} = \omega_{LO} - \omega_{image}$$

- **Image**
  - **Mirror-like symmetry about the LO**
  - **Undesired signal, noise**
  - **Suppressed by filtering**

Mixer



- ❑ RF – V-I converter
- ❑ LO – alternating switches
- ❑ R – load

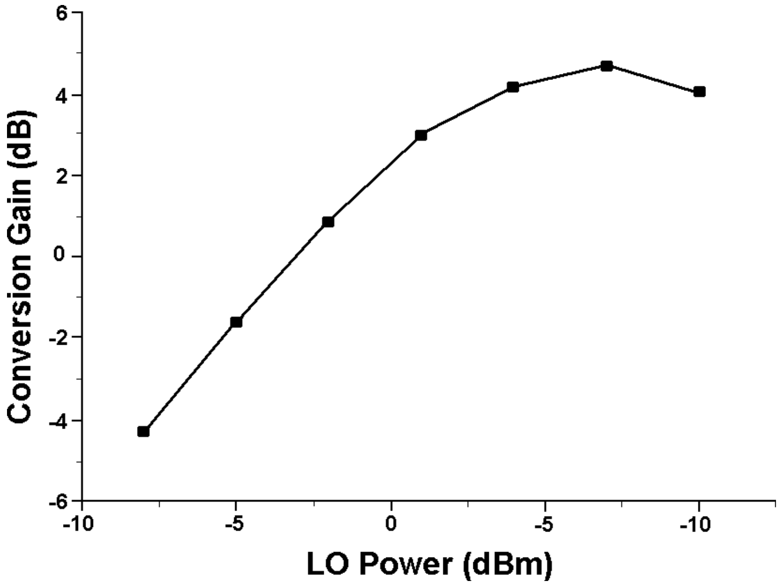
Design Considerations

- Input and Output Impedance
- Conversion Gain
- Noise Figure
- Linearity
  - 1dB Compression Point
  - IIP3
- Isolation
- LO Input Power

Input and Output Impedance

- LNA and mixer – directly connected at low-IF
- On-chip connection << wavelength of signal
- Input matching
  - Needed for stand-alone mixers
  - Zin (mixer) = Zout (source)
  - S11 < -10dB – sufficient for practical applications
- Output matching
  - Zout (mixer) = Zin (measuring device)
  - Buffer

Conversion Gain



$$VoltageGain = 20\log\left(\frac{V_{out}}{V_{in}}\right)$$

$$PowerGain = 10\log\left(\frac{P_{out}}{P_{in}}\right)$$

$$PowerGain = VoltageGain - 10\log\left(\frac{R_S}{R_L}\right)$$

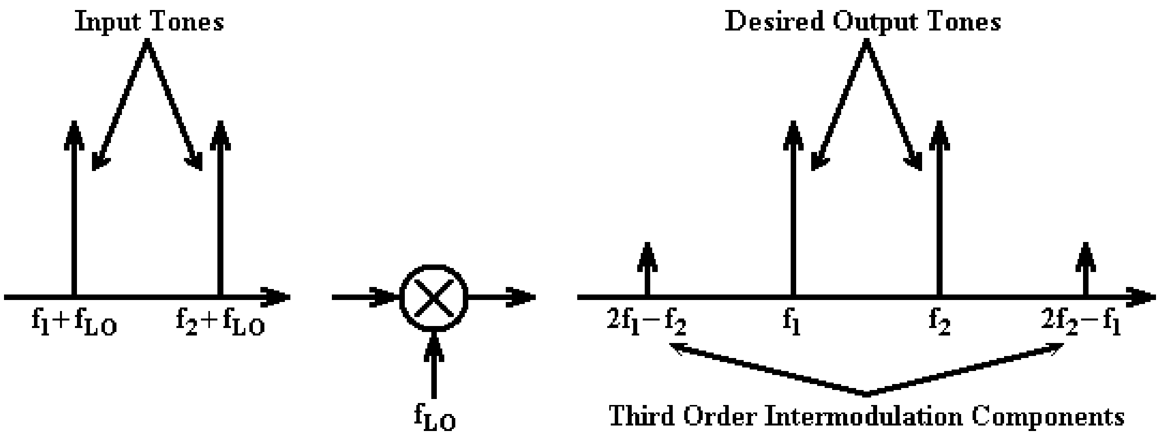
- Efficiency of the transposition from RF to IF
- Ratio of IF output versus RF input
- Affects the linearity & NF of the receiver

Noise Figure

$$NF = 10\log\left(\frac{SNR_{IN}}{SNR_{OUT}}\right) = 10\log\left(\frac{N_s + N_a}{N_s}\right)$$

- **Input noise corruption relative to output noise corruption measured in decibels**
- **Both RF signal and image signal contributes output noise**
- **SSB NF – noise to be measured at low-IF**

Linearity



$$S_{out}=a_0+a_1 S_{in}+a_2 S_{in}^2+a_3 S_{in}^3+a_4 S_{in}^4+\ldots$$

$$S_{in}=x_1+x_2=A_1\cos\omega_1 t+A_2\cos\omega_2 t$$

$$S_{out}=a_0+a_1(x_1+x_2)+a_2(x_1+x_2)^2+a_3(x_1+x_2)^3$$

$$S_{out}=a_0+a_1(x_1+x_2)+a_2(x_1^2+2x_1x_2+x_2^2)+a_3(x_1^3+3x_1^2x_2+3x_1x_2^2+x_2^3$$

Linearity

$$(x_1+x_2)^2 = a_2(x_1^2 + 2x_1x_2 + x_2^2)$$

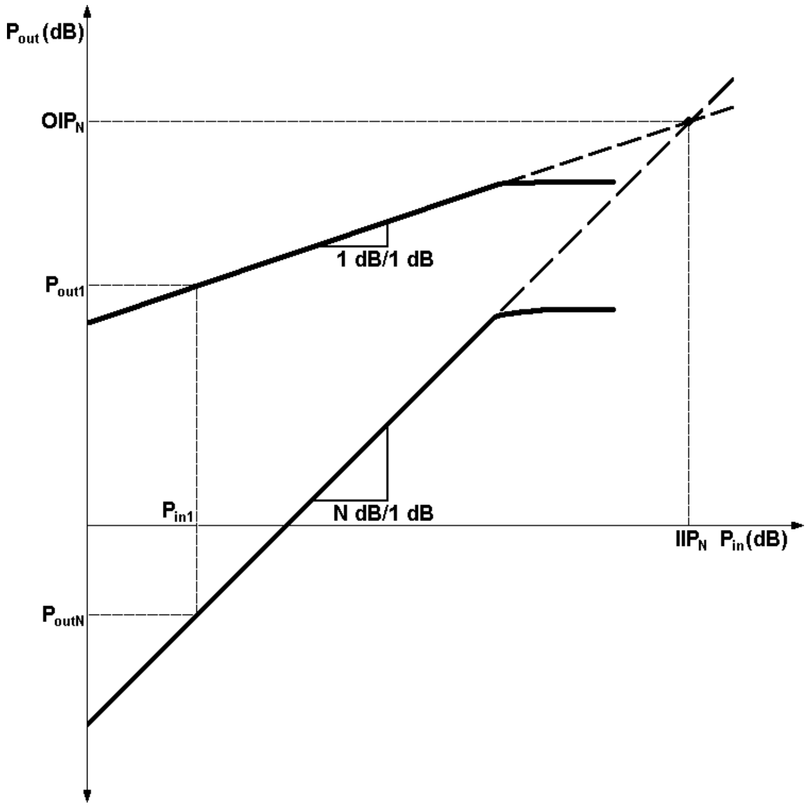
HD2 MIX HD2

$$(x_1+x_2)^3 = (x_1^3 + 3x_1^2x_2 + 3x_1x_2^2 + x_2^3)$$

HD3 IM3 IM3 HD3

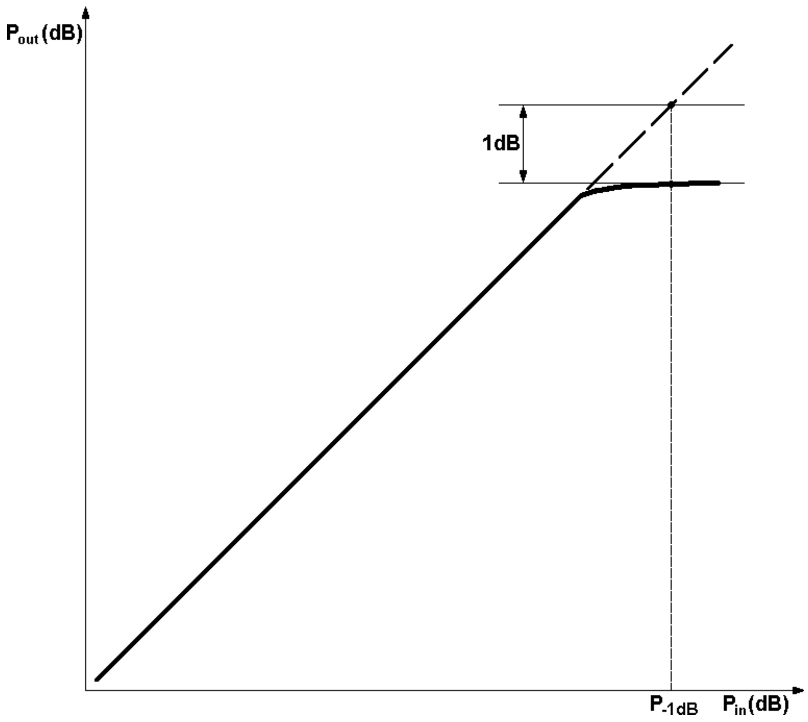
- **MIX (IM2) – for frequency translation**
- **HD3 & IM3 – gain compression and intermodulation distortion**

IIP3



- Commonly used measure of linearity
- Intersection of output power of the desired signal and the IM3
- IIP3 – referred to the input power
- OIP3 – referred to the output power

1dB Compression Point



- Used to estimate the largest input possible
- 1dB decreased in gain from ideal
- Large signal input conditions
- $P_{-1\,dB} = IIP_3 - 9.6\,dB$

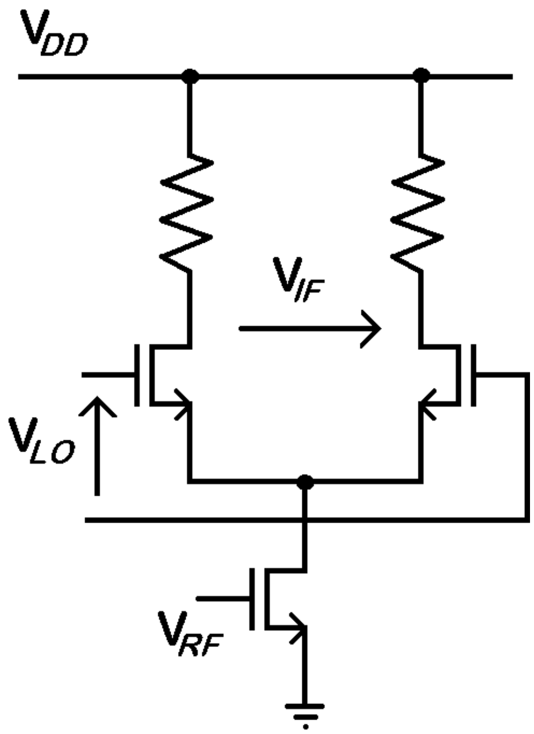
Isolation

- LO to RF
  - Quite serious in zero-IF architectures
  - DC offsets
- LO to IF
  - Degrads the performance of the following stage
- RF to IF
  - Critical issue in zero-IF architectures

Mixer Topologies

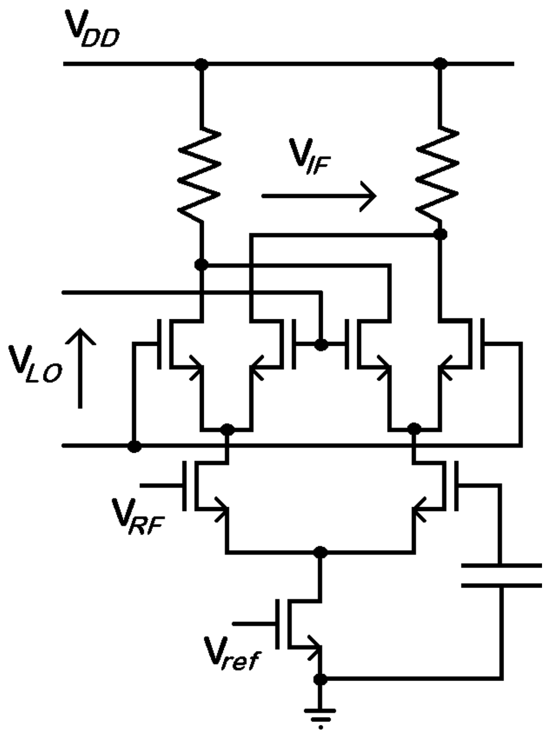
- Passive
- Active
  - Single-balanced Mixer
  - Double-balanced Mixer
  - CG-CS Mixer
  - Folded Switching Mixer

Single-balanced Mixer



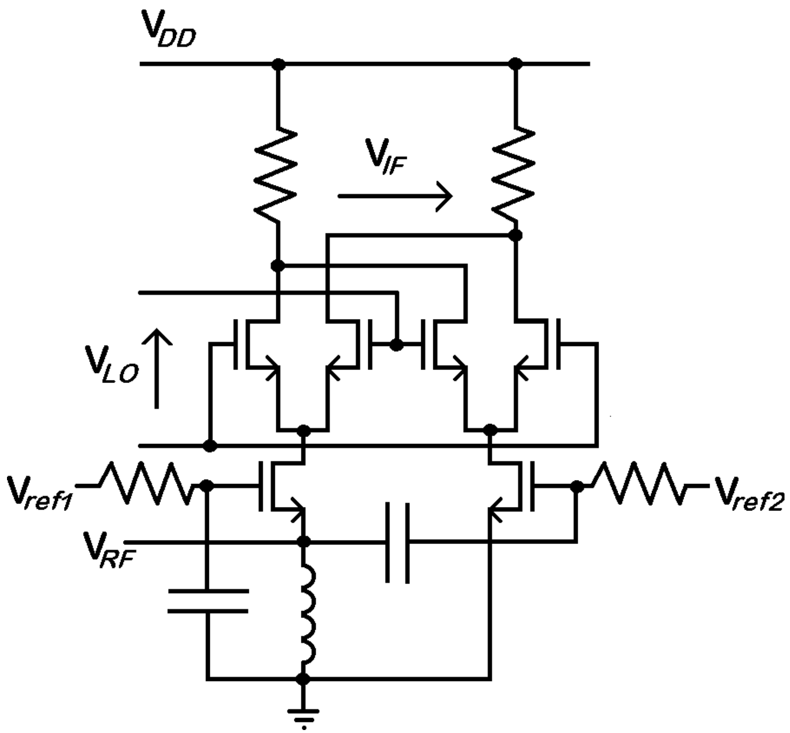
- Simplest active mixer
- Single-ended RF input
- Moderate gain
- Low NF
- Low IIP3, 1dB CP, Isolation
- High input impedance

Double-balanced Mixer



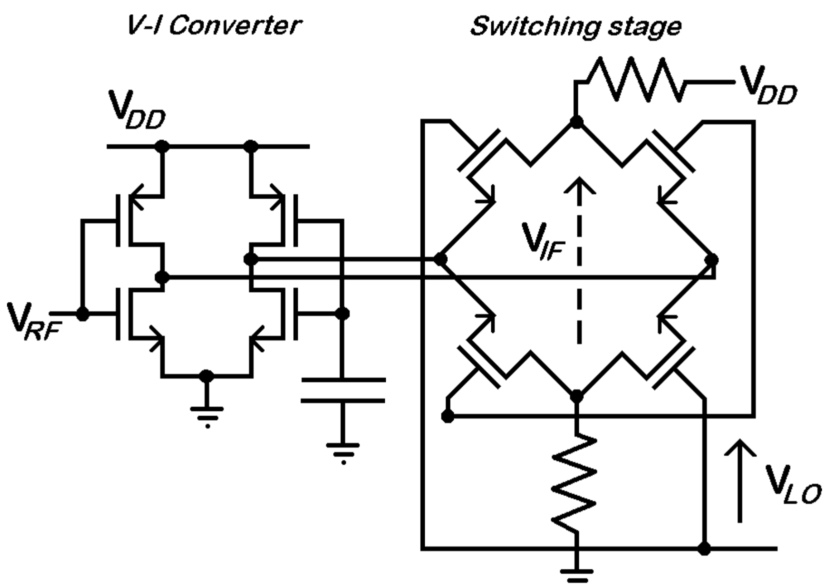
- Gilbert cell
- Symmetrical
  - High Isolation
  - Output Rejection
- High gain
- Very low NF
- Good linearity

CG-CS Mixer



- 2 input transistors
  - Common-gate
  - Common-source
- Single-to-differential
- High IIP3
- Modest NF

Folded Switching Mixer

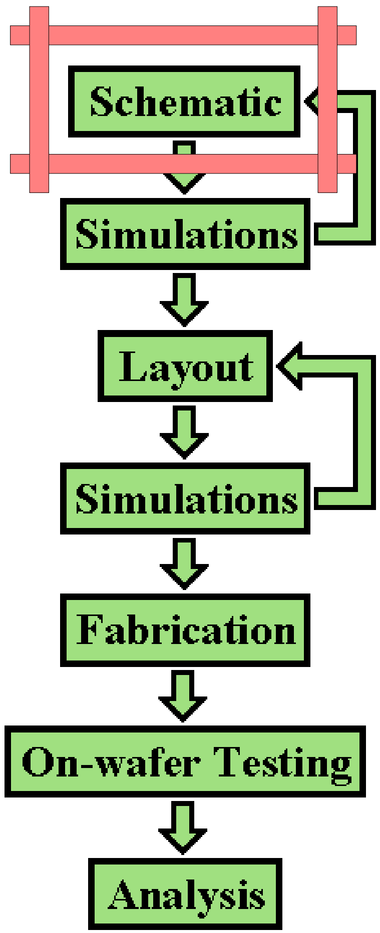


- High gain at low voltage supply
- Low NF
- Moderate linearity
- Low power

Statement of the Problem

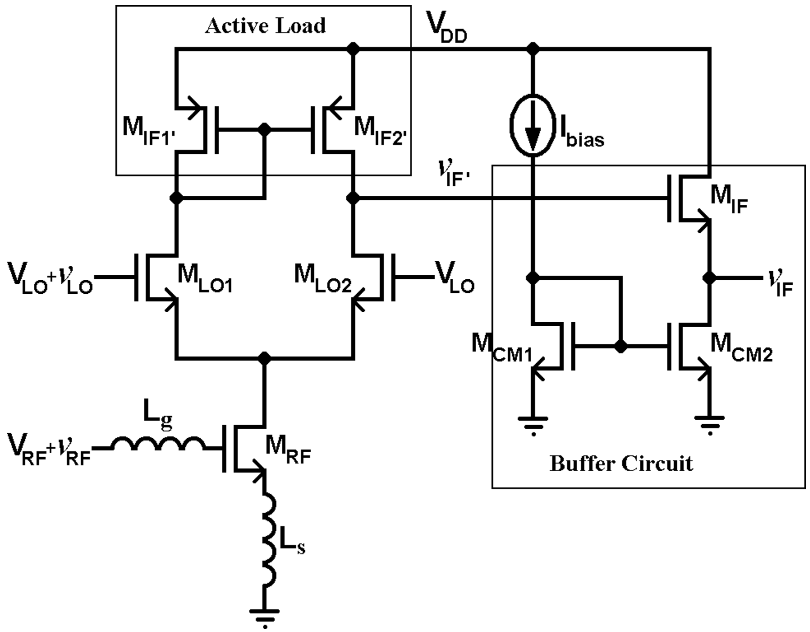
A clear guideline in designing low-IF RF CMOS mixers are unavailable. Data on the different performance parameters are inadequate and hard to quantify. In response to these shortcomings, this study aims to develop a methodology in the design and testing of RF CMOS mixers to maximize time, effort and money.

Methodology



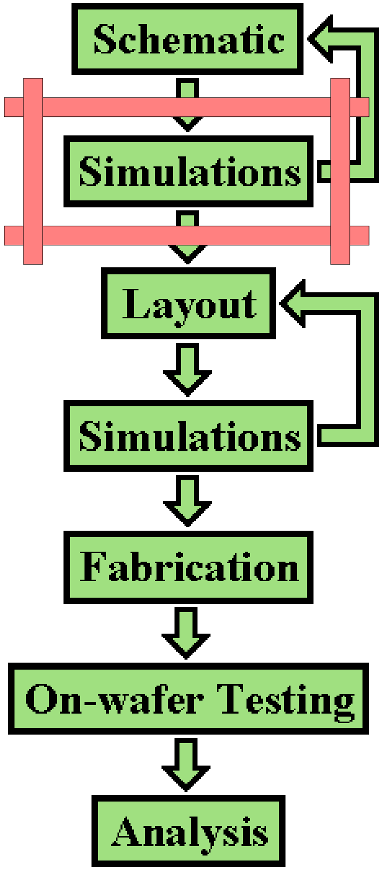
- Cadence Schematic Editor
- Reference Circuit
  - Single-ended
    - LO input
    - IF output
  - Active Load
  - Buffer Circuit
  - Inductors

Reference Circuit



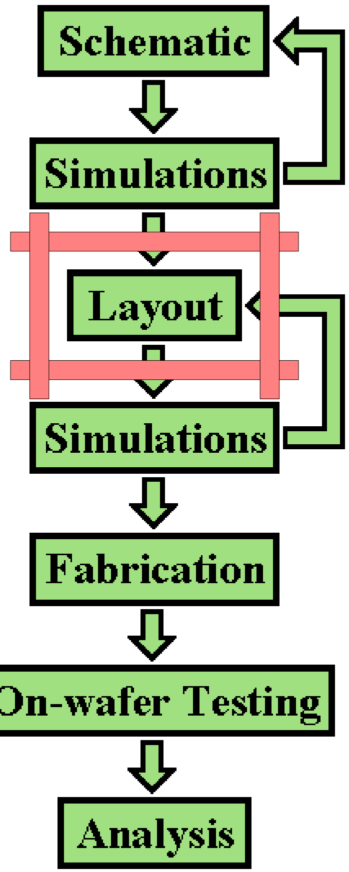
- Design Metrics
  - g_m/I_d
  - Inductor types
  - Transistor sizes
    - RF
    - LO
    - Load
- Impedance Matching
  - Input – Inductor
  - Output – Buffer

Methodology



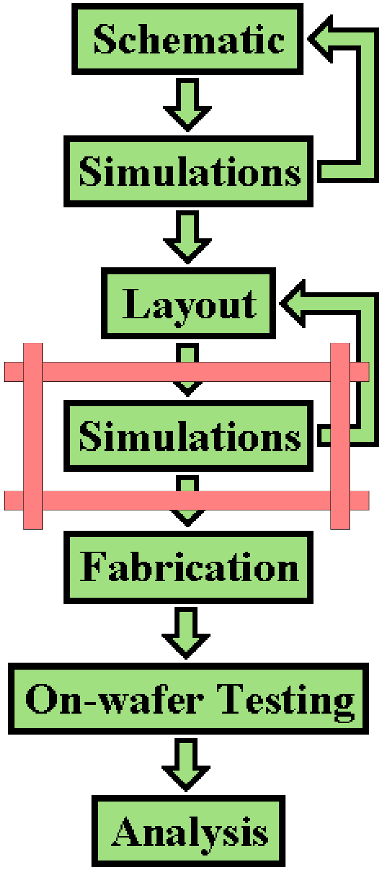
- Simulations
  - SpectreRF by Cadence
- Analysis
  - DC – DC operating pts.
  - SP – S11parameters
  - PAC – Conversion Gains
  - PAC, Pnoise – NFs
  - PAC, PSS – IIP3, 1dB CP
- ASITIC

Methodology



- Cadence Virtuoso Layout Editor
- 0.25 μm CMOS
- Transistor
  - Cluster of finger
  - Double-contacted gate
- Inductor
  - Metal 4 & Metal 5

Methodology



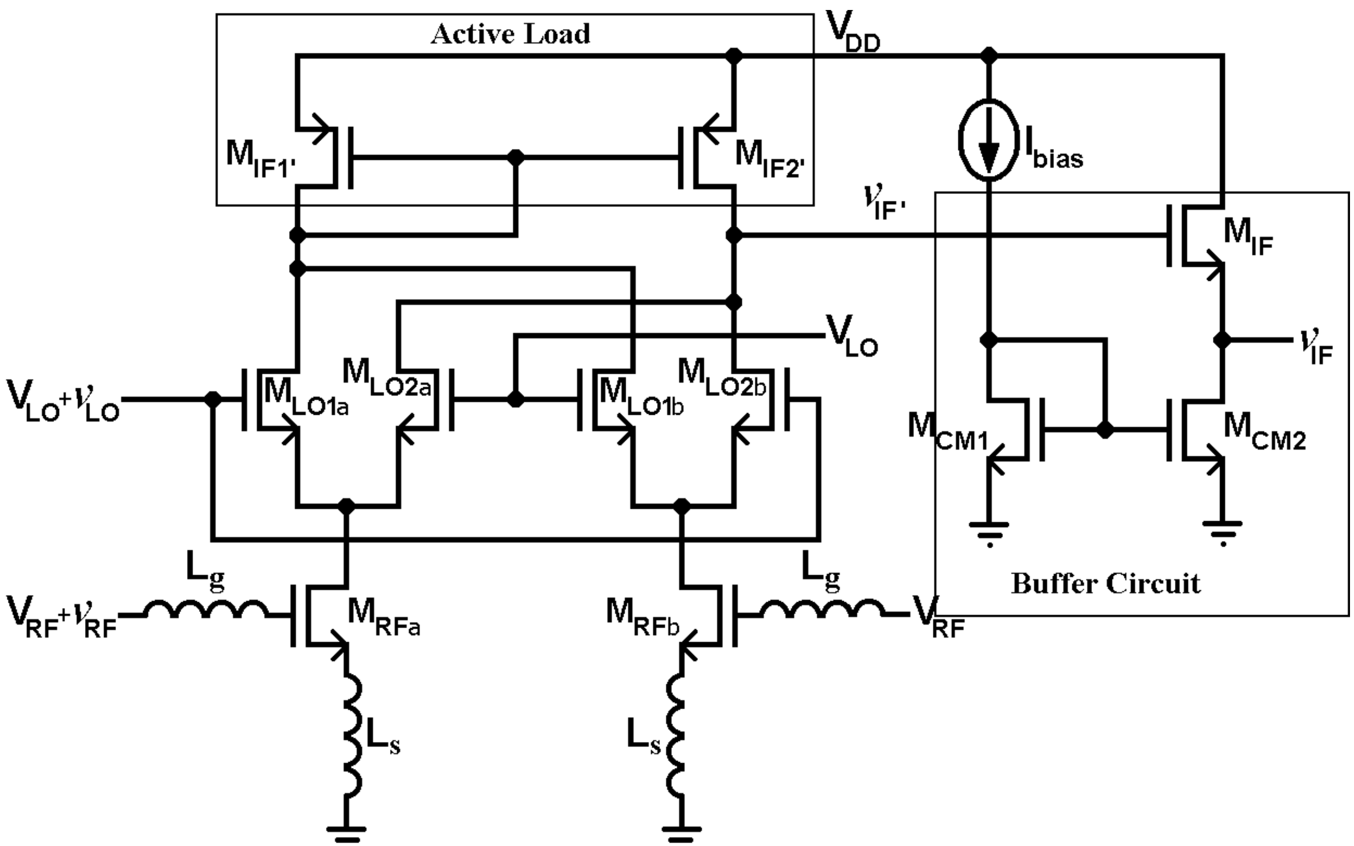
- Simulations
  - SpectreRF by Cadence
- 13 Test Structures
  - 11 Single-balanced Mixers
  - 1 Double-balanced Mixer
  - 1 Open Structure

List of Test Structures

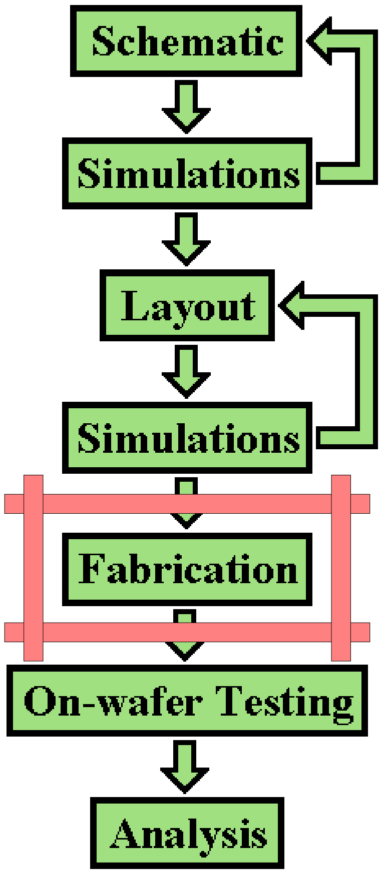
Test Structure	g_m/I_D	RF Width (mm)	LO Width (mm)	Conversion Gain (dB)	Inductor Type
*single 1	10	300	300	6	square
*single 2	10	250	300	6	square
*single 3	10	350	300	6	square
single 4	10	300	150	6	square
single 5	10	300	450	6	square
single 6	10	300	300	3	square
*single 7	10	300	300	9	square
*single 8	10	300	300	6	halo
*single 9	10	300	300	6	PGS
single 10	5	300	300	6	square
single 11	15	300	300	6	square
double	10	300	300	6	square
*open	-	-	-	-	-

***Sent for fabrication: 23 August 2004*

Double-balanced Mixer

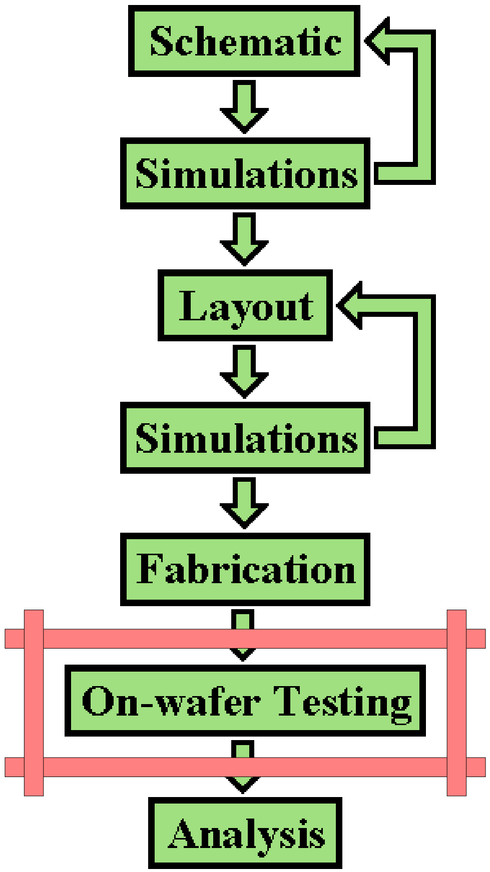


Methodology



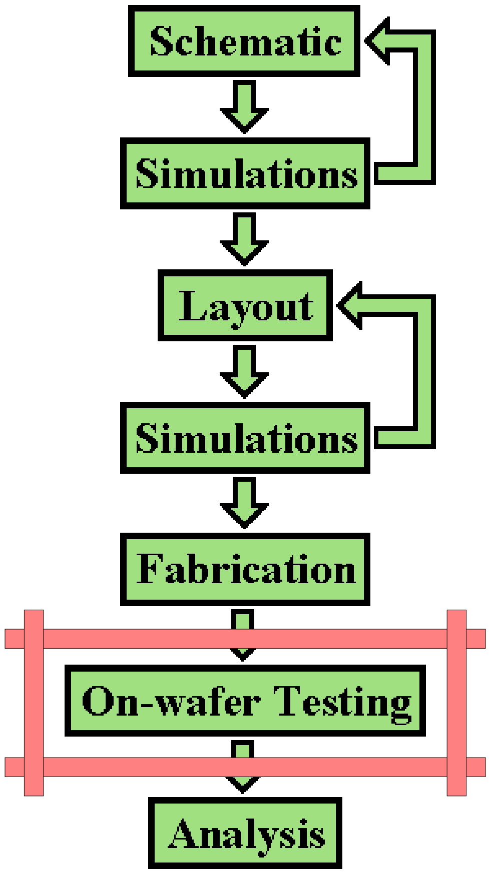
- Fabricated
  - TSMC
  - 1st Fab: Aug 23, 2004
    - 7 Test Structures
  - 2nd Fab: Jan-Feb 2005

Methodology



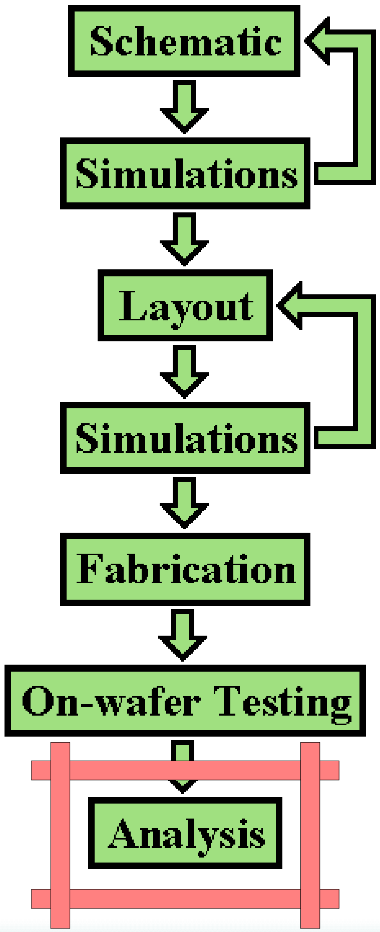
- Micromanipulator
- GSG probes
- Parametric Analyzer
  - DC supply
  - Measure DC
- Signal Generator
  - AC supply (RF & LO)

Methodology



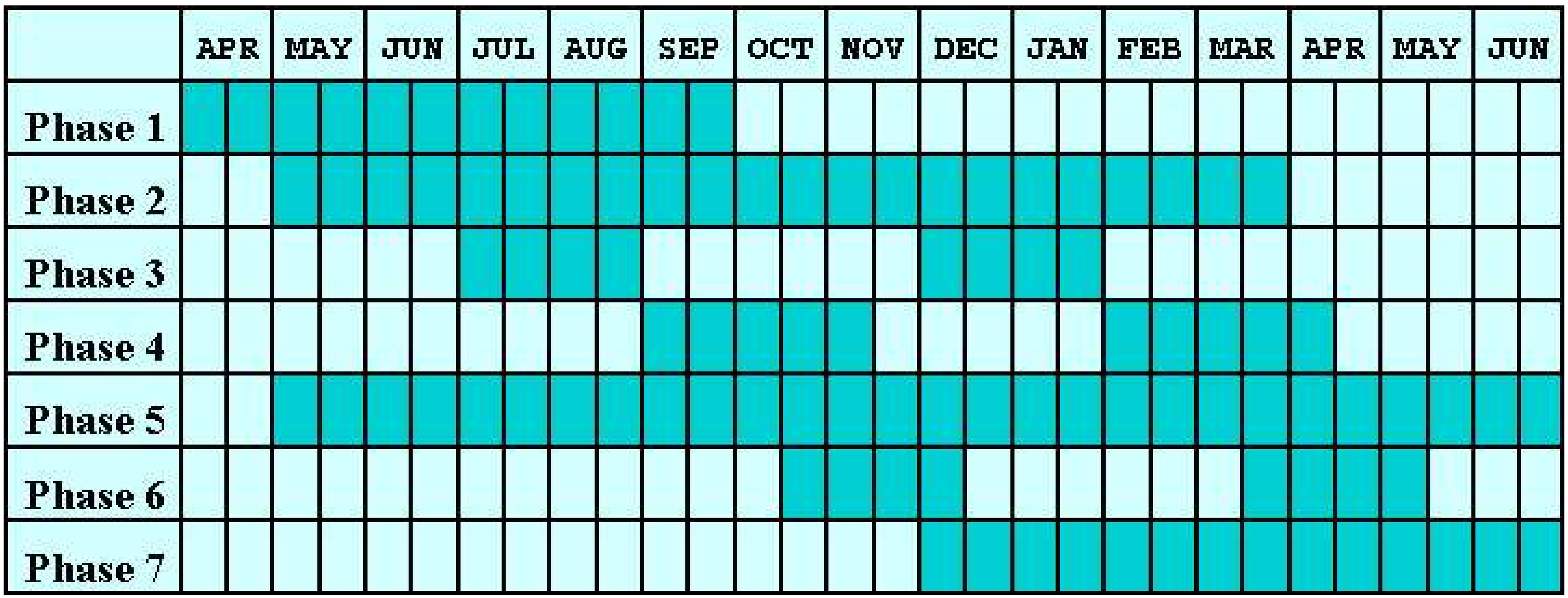
- Network Analyzer
  - S Parameters
- Spectrum Analyzer
  - Conversion Gain
  - Noise Figure
  - IIP3
  - 1dB Compression Point

Methodology



- Data Gathering
- Collation
- Analysis
- Conclusions
- Recommendations

Gantt Chart



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Phase 1
Phase 2
Phase 3
Phase 4
Phase 5
Phase 6
Phase 7

Schedule

- Phase 1 – Gathering of material and literature review
  - Thesis proposal.
- Phase 2 – Simulation and initial data gathering
  - Testing methodology for mixers.
  - Collated data needed in the actual mixer design and implementation.
- Phase 3 – Mixer Design and Implementation
  - Fabrication ready mixer test structures.
- Phase 4 – Chip fabrication

Schedule

- Phase 5 – Documentation
  - Paper documentation.
- Phase 6 – On-wafer Testing
  - Methodology for mixer testing.
  - Data of fabricated mixers.
- Phase 7 – Analysis and Results
  - Analysis on the data gathered.
  - Conclusions on the impact of varying device sizes and design parameters.
  - Recommendations for future works on mixers.

Summary

- Aims to develop a methodology in designing and testing of low-IF RF CMOS mixers.
- 13 test structures will be fabricated & characterized.
- Measure the following parameters:
  - DC characteristics
  - S Parameters
  - Conversion gain versus LO input power.
  - Noise figure versus LO input power.
  - 1 dB compression point
  - IIP3

Thank You!

Receiver Architectures

- **High-IF (Superheterodyne system)**
  - **High-Q components – superior sensitivity and selectivity**
  - **Low level of integration**
- **Zero-IF (Direct conversion)**
  - **High level of integration**
  - **Flicker noise, DC offsets, high sensitivity to 2^{nd} order distortion**

Receiver Architectures

- Low-IF
  - Typically few MHz
  - Flicker noise and DC offsets are avoided
  - High level of integration
  - Bluetooth